IN THE SPECIFICATION

Please replace the paragraph at page 7, lines 6-17, with the following rewritten paragraph:

A fourth aspect of the present invention is the driving method of a self-luminous display apparatus according to ~~any one of~~ the first ~~to the third aspects~~ aspect of the present invention, wherein the applied amount of current is determined by acquiring a current value i1 which is a maximum value of the image data inputted from outside in a first period, acquiring a proper current value i2 by calculation from the image data inputted in a second period, and sequentially calculating the amount of current applied to each of the pixels displayed based on the predetermined image data inputted in the second period based on a ratio i2/i1.

Please replace the paragraph at page 7, line 18, to page 8, line 5, with the following rewritten paragraph:

A fifth aspect of the present invention is the driving method of a self-luminous display apparatus according to ~~any one of~~ the first ~~to the third aspects~~ aspect of the present invention, wherein the applied amount of current is determined by acquiring a third current value i3 which is a maximum value of the inputted image data, actually applying a current between the anode and the cathode of each of the self-luminous display elements, acquiring an optimum value as a second current value i4 and multiplying the inputted image data by a ratio i4/i3 and thereby sequentially calculating the amount of current applied to each of the pixels displayed based on the predetermined image data.

Please replace the paragraph at page 8, lines 6-15, with the following rewritten paragraph:

A sixth aspect of the present invention is the driving method of a self-luminous display apparatus according to ~~any one of~~ the first ~~to the third aspects~~ aspect of the present invention, wherein the gradation value of the video data inputted from outside is on a higher gradation side of performing a white display than the first predetermined gradation value, and the amount of current applied between the anode and the cathode of each of the self-luminous elements is controlled by a black insertion rate.

Please replace the paragraph at page 9, lines 10-20, with the following rewritten paragraph:

A tenth aspect of the present invention is the driving method of a self-luminous display apparatus according to ~~any one of~~ the first ~~to the third aspects~~ aspect of the present invention, wherein the gradation value of the video data inputted from outside is on a higher gradation side of performing a white display than the first predetermined gradation value, and the amount of current applied between the anode and the cathode of each of the self-luminous elements is controlled by adjusting the amount of current passing through a group of source lines.

Please replace the paragraph at page 10, lines 9-20, with the following rewritten paragraph:

A thirteenth aspect of the present invention is the driving method of a self-luminous display apparatus according to ~~any one of~~ the first ~~to the third aspects~~ aspect of the present invention, wherein a difference between a first current passing between the anode and the cathode of each of the self-luminous elements in a first frame period and a second current

passing in a second frame period following the first frame period is acquired, an n difference current value of which difference value is 1/n (n is a number of 1 or more) is calculated, and a selection value of a pixel line is determined from the n difference current value.

Please replace the paragraph at page 11, lines 1-7, with the following rewritten paragraph:

A fifteenth aspect of the present invention is the driving method of a self-luminous display apparatus according to ~~any one of~~ the first ~~to the third aspects~~ aspect of the present invention, wherein a γ constant is corrected to be optimum by the amount of current passing between the anode and the cathode of each of the self-luminous elements.

Please replace the paragraph at page 11, line 20, to page 12, line 5, with the following rewritten paragraph:

An eighteenth aspect of the present invention is the driving method of a self-luminous display apparatus according to ~~any one of~~ the first ~~to the third aspects~~ aspect of the present invention, wherein on and off of the second process is controlled by placing switching instrument for the second processing instrument so as to determine the amount of current passing between the anode and the cathode of each of the self-luminous element by combining the first process and the second process when turned on and determine it only by the first process when turned off.

Please replace the paragraph at page 15, lines 19-25, with the following rewritten paragraph:

A twenty-fifth aspect of the present invention is the driving circuit of the self-luminous display apparatus according to ~~any one of~~ the nineteenth ~~to the twenty-fourth~~

~~aspects~~ aspect of the present invention, comprising switching instrument for the second processing instrument which has operations effected only by the first processing instrument.

Please add the following new paragraph at page 15, after line 25:

A twenty-sixth aspect of the invention is the driving circuit of the self-luminous display apparatus according to the twentieth aspect of the present invention, comprising switching instrument for the second processing instrument which has operations effected only by the first processing instrument.

Please replace the paragraph at page 16, lines 1-5, with the following rewritten paragraph:

A ~~twenty-sixth~~ twenty-seventh aspect of the present invention is the controller of the self-luminous display apparatus having the driving circuit according to ~~any one of~~ the nineteenth ~~to the twenty-fourth aspects~~ aspect of the present invention.

Please add the following new paragraph at page 16, between lines 5 and 6:

A twenty-eighth aspect of the invention is the controller of the self-luminous display apparatus having the driving circuit according to the twentieth aspect of the present invention.

Please replace the paragraph at page 16, lines 6-12, with the following rewritten paragraph:

A ~~twenty-seventh~~ twenty-ninth aspect of the present invention is the self-luminous display apparatus comprising the driving circuit according to ~~any one of~~ the nineteenth ~~to the twenty-fourth aspects~~ aspect of the present invention, in which the self-luminous elements are formed or placed like a matrix in the pixel row direction and the pixel line direction.

Please add the following new paragraphs at page 16, between lines 12 and 13:

A thirtieth aspect of the invention is the self-luminous display apparatus comprising the driving circuit according to the twentieth aspect of the present invention, in which the self-luminous elements are formed or placed like a matrix in the pixel row direction and the pixel line direction.

A thirty-first aspect of the present invention is a driving method of a self-luminous display apparatus having a plurality of self-luminous elements comprising each of pixels placed like a matrix in a pixel row direction and a pixel line direction and driving a display portion by passing a current between an anode and a cathode of each of the self-luminous elements and thereby emitting light from each of the pixels, wherein:

the light is emitted from the display portion by controlling an amount of current passing each of pixel lines based on results of (1) a first process of acquiring a first amount of current to be passed between the anode and the cathode correspondingly to video data inputted from outside, and acquiring a predetermined single value as the first amount of current irrespective of a status of video data value distribution around the video data or (2) a second process of acquiring a second amount of current to be passed between the anode and the cathode correspondingly to the video data inputted from outside; and preparing as the second amount of current a value having the first amount of current suppressed at a predetermined ratio according to the status of video data value distribution around the video data while the ratio of suppression being variable according to the status of video data value distribution, and

in the case where the amount of current equivalent to displaying white is represented as 100, and if a gradation of a low-current region having the predetermined amount of current represented as 30 or less is given a positive number which is $N1 > 1$, $N2 > 0$ and $N1 \geq N2$ as

a coefficient, W as the predetermined amount of current, I org as a current value at the time, and T org as a light emitting period, the amount of current satisfying the current value of I org x N1 and the light emitting period of T org x 1/N2 is applied instead of the predetermined amount of current.

Please replace the paragraph at page 25, lines 7-9, with the following rewritten paragraph:

Figure 106 is a diagram showing a relationship between the input data and the number of lighting horizontal ~~operating~~ scanning lines;

Please replace the paragraph at page 25, lines 12-14, with the following rewritten paragraph:

Figure 108 is a diagram showing a relationship between the input data and the number of lighting horizontal ~~operating~~ scanning lines;

Please replace the paragraph at page 25, lines 15-16, with the following rewritten paragraph:

Figure [[107]] 109 is a diagram showing the relationship between the input data and the temperature rise;

Please replace the paragraph at page 51, line 15, to page 51, line 2, with the following rewritten paragraph:

Therefore, the off voltage of the gate (Vgh, that is, a voltage side closer to the power supply voltage in Figure 1) should be ~~than in~~ the range of – 0.5 (V) to + 4 (V) to the power supply voltage (Vdd of Figure 1). More desirably, it should be ~~than in~~ the range of 0 (V) to +

2 (V) to the power supply voltage (Vdd of Figure 1). To be more specific, the off voltage of the transistor applied to the gate signal line should be sufficiently off. In the case where the transistor is on the N channel, Vg1 becomes the off voltage. Therefore, Vg1 should be in the range of – 4 (V) to 0.5 (V) to the GND voltage. More desirably, it should be in the range of -2 (V) to 0 (V).

Please replace the paragraph at page 71, line 3, to page 72, line 9, with the following rewritten paragraph:

It is also desirable to increment the input data by 2 raised to n-th power between the minimum and the maximum. For instance, it is a method whereby total white lighting is 256 (2 raised to 8-th power) if total black lighting is 0. To acquire a change amount when calculating a change in the lighting rate, it is necessary to divide a maximum lighting rate and a minimum lighting rate by the input data. Incorporating a dividing circuit in semiconductor design is a very large load in the circuit configuration. When doing so, it is possible, by defining the total white display as 2 raised to n-th power, to acquire inclination just by shifting the difference between the maximum lighting rate and the minimum lighting rate by 8 bits as a binary number. Therefore, it is no longer necessary to incorporate the dividing circuit considering it from a view point of the semiconductor design so that circuit design becomes very easy. When implementing a waveform of gradually lowering the lighting rate after keeping the maximum lighting rate for a certain period as indicated by reference numeral 291, the waveform of which lighting rate becomes maximum in the period from the minimum to 2 raised to n'-th power of the input data as shown in Figure 30 intersects with a dotted linear graph ~~such as ()~~ if, when the inclination is x, the inclination is 2x only in the period from 2 raised to n'-th power to 2 raised to (n'+1-th power). Using this structure, it is no longer necessary, just by acquiring the linear inclination, to acquire the inclination again

on rendering it as a line plot. Therefore, it is possible to create various line plots without enlarging a circuit scale. This has a merit of constituting a small circuit scale in the circuit design.

Please replace the paragraph at page 72, line 10, to page 74, line 2, with the following rewritten paragraph:

Subsequently, a description will be given by using Figure 55 as to the circuit configuration of implementing this drive. First, color data of RGB is inputted to 551 by a video source. The same data is inputted to the source driver IC 14 after undergoing image processing such as a γ process. Figure 55 describes the color data of RGB. However, it is not limited to RGB. It may be the signal of YUV or may be temperature data or luminance data obtained from the aforementioned thermistor and photo sensor. After expanding the data in 551, the data is inputted to a module 552 of collecting the data. Expansion of the data in 551 will be described later. In the module 552, the data is inputted to an adder 552a first. However, the data is not always there, but indefinite data other than the image data may be there in some cases. For that reason, the adder 552a decides whether or not to perform addition depending on an enable signal (DE) of whether or not the data is there and a clock (CLK). However, the enable signal is not necessary in the case of the circuit configuration in which no data other than the image data is inputted. The added data is stored in a register 552b. And 552c latches it with a vertical synchronizing signal (VD) and outputs high-order 8 bits of the data (binary number) of the register. The size of the register is not defined. The larger the size of the register is, the larger the circuit scale becomes while the accuracy of the additional data is improved. The outputted data is not fixed to 8 bits. The outputted data may be 9 bits or more when controlling the lighting rate in a finer range, and may be 7 bits or less when accuracy ~~does not require~~ is not required. The maximum value of the outputted values

is an increment of the inputted data. In the case where the maximum value of the outputted 8 bits is 100, the inputted data is determined by dividing it into 100. It is desirable to increment the input data by 2 raised to n-th power in order to reduce the circuit scale as previously mentioned. Thus, in 551, the data is expanded in order to make it easy to equally divide the data obtained among 1F into 255. If the outputted value becomes 100 at the maximum when the data is inputted as-is to 552, the input data itself is multiplied by 2.55 in 551 and then inputted so that the maximum outputted value can become 255 (256 (2 raised to 8-th power) including 0).

Please replace the paragraph at page 76, line 16, to page 77, line 23, with the following rewritten paragraph:

Figure 59 shows the relationship between the number of necessary frames and s when the lighting rate shifts from 0 to 100. In the case where the video shows at a frequency of 60 Hz, it requires approximately 200 frames at s 32 until the lighting rate shifts to 100 percent from 0 percent, which takes about 3 seconds. If the change takes longer than this, the change in brightness cannot be smoothly seen on the contrary. If s is small, the flicker cannot be improved. As the data is described as binary numbers in the circuit design, the dividing circuit requires a lot of logic. Therefore, implementation thereof is not realistic. When dividing by 2 raised to n-th power, however, the circuit configuration becomes very easy because the same effect as division can be obtained just by shifting to the right by n bits if a leftmost bit of the data described as binary numbers is the highest-order bit and a rightmost bit thereof is the lowest-order bit. From the aforementioned viewpoint, s should be 2 raised to n-th power. Figure 134 shows the change of the lighting rate on shifting from a ~~front~~ total black display status to a ~~front~~ total white display. As a result of examination, there is little improvement effect in the case of s = 2 while the flicker is improved in the case of s = 4. If it

exceeds s = 256, the change takes such a long time that it no longer works as a suppression function. Considering the above, the range of s is $4 \leq s \leq 256$ according to the present invention. It should preferably be $4 \leq s \leq 32$. It was thereby possible to obtain a good display with no flicker. Apart from the circuit design, s is not limited to 2 raised to n-th power. When multiplying the numerator (Y'(t) – Y(t)) of (Y'(t) – Y(t))/s of formula (5) by r, the range of s is also multiplied.

Please replace the paragraph at page 78, line 12, to page 79, line 5, with the following rewritten paragraph:

Figure 58 shows a circuit configuration of the driving method of delaying the change of the lighting rate. As previously described, the data outputted from 551 is added by the adder 552a, and is stored in the register 552b. The value of 8 bits outputted in synchronization with VD is calculated by a calculation module so as to derive a lighting rate control value Y'(t). Y'(t) is inputted to a subtraction module 582. In the subtraction module 582, a subtraction is performed between a lighting rate control value Y(t) obtained from a register 583 holding a current lighting rate control value and the lighting rate control value Y'(t) derived from the current input data so as to acquire a difference S(t) between the two. Next, S(t) is divided by the value of inputted s inside 584. ~~For use~~ As previously described, the division requires complicated logic. Therefore, the inputted s is raised to n-th power, and it thereby becomes possible to divide S(t) by shifting to the lowest-order bit (LSB) side by n bits.

Please replace the paragraph at page 79, line 13, to page 80, line 8, with the following rewritten paragraph:

In the case of the method of Figure 58, however, the data equivalent to the amount of the shift is discarded on shifting S(t) by n bits and so there arises a problem as to the accuracy. To be more precise, in the case of s = 8, it is n = 3 so that S(t) is shifted by 3 bits. In the case where S(t) is a numerical value of 7 or less, however, it becomes 0 if shifted to the LSB side by 3 bits. To avoid this, both S(t) and Y(t) are shifted to the highest-order (MSB) bit side by n bits in advance, and on outputting, output data is shifted to the LSB side by n bits and then outputted. Or else, an initial value Y(0) is ~~done~~ shifted to the MSB side by n bits and then stored in the register 583 ~~for use~~ as shown in Figure 61. And the data on adding S(t) is stored in the register 583 while the output data is shifted to the LSB side by n bits and then outputted. As the initial value is shifted to the MSB side by n bits, S(t) which is added can have the same effect as being shifted to the LSB side by n bits. Furthermore, the data to be stored in the register 583 has no data to be discarded by the shift. Thus, the accuracy is improved.

Please replace the paragraph at page 85, lines 11-19, with the following rewritten paragraph:

Thus, two signal ~~battles~~ lines 62a and 62b are placed in the gate driver IC 12 as shown in Figure 6. The two signal lines 62a and 62b are connected to gate control signal lines 64 and OR circuits 65 connected to the shift registers. The output of the OR circuits 65 is connected to output buffers 63, and is then outputted to the gate signal lines 17. As shown in Figure 28, the gate signal lines 17 output LOW only when both the signal lines 62 and 64 are LOW, and output HI when one of them is HI.

Please replace the paragraph at page 89, line 24, to page 90, line 11, with the following rewritten paragraph:

As this driving is performed in the period in which the lighting rate is $N/S \leq 1/4$, the lighting rate control value 556 is inputted from 555 to 601. 601 performs the driving at the lighting rate of $N/S \leq 1/4$. As previously indicated, the signal line 62b outputted from 601 has the logical operation performed with a signal line 64b outputted from the gate driver IC 12, and the output thereof is the gate signal line 17b. For this reason, it is possible to operate the transistors 11d of all the pixels in an output status of the signal line 62b. In a section of $N/S \geq 1/4$ performing no driving, output is produced to the signal line 62b ~~for use~~ so as to reflect an output waveform of the signal line 64b on 17b.

Please replace the paragraph at page 90, line 12, to page 91, line 2, with the following rewritten paragraph:

In the case of $N/S \leq 1/4$, 601 drives in synchronization with an HD. It does not necessarily synchronize only with the HD. It is also feasible to provide a dedicated signal of driving 601. 601 operates the signal line 62b so that the transistors 11d are turned off for a specified period by an inputted fine-tuning signal 602 and a clock (CLK). ~~For use~~ As previously indicated, if the HI output period of the signal line 62b in one horizontal period (1H) is M (μ) in the status of lighting up N lines, the lighting time of one inter-frame space decreases by $M \times N$ (μ). For that reason, it is possible to calculate M by calculating the time of 1H and the data of 602 and manipulate reduction in the lighting time by the operation of the signal line 62b so as to change the lighting rate smoothly.

Please replace the paragraph at page 97, lines 4-22, with the following rewritten paragraph:

Thus, it is proposed to use the driving method of controlling the lighting rate according to the input data of the present invention and thereby control the lighting rate and the amount of current passing through the source signal line 18 in the low luminance portion of a display image so as to perform the N-times pulse drive only in the low luminance portion as shown in Figure 49. This driving method has a merit that, since the aforementioned problem of shortage of the amount of current hardly arises in a high luminance portion. ~~For that reason~~, the N-times pulse drive placing a burden on the EL element 15 is not performed in the high luminance portion but performed only in the low luminance portion having less current passing through the pixels on the whole[[. It]], and hence it is thereby possible, while reducing the burden on the organic EL element, to solve the aforementioned problem that the signal before changing to the predetermined luminance is written inside the pixels for the stray capacitance 451 of the source signal line.

Please insert the following new paragraph at page 98, between lines 21 and 22:

To be more specific, in the case where the amount of current equivalent to displaying white is represented as 100, and if a gradation of a low-current region having the predetermined amount of current represented as 30 or less is given a positive number which is $N1 > 1$, $N2 > 0$ and $N1 \geq N2$ as a coefficient, W as the predetermined amount of current, I org as a current value at the time, and T org as a light emitting period, the amount of current satisfying the current value of I org x N1 and the light emitting period of T org x 1/N2 is applied instead of the predetermined amount of current.

Please replace the paragraph at page 100, line 23, to page 101, line 11, with the following rewritten paragraph:

The source driver 14 will be described by referring to Figures 62 and 63. ~~For use~~ As shown in Figure 63, the source driver 14 passes the current through the source signal line 18 according to a reference current 629. To further describe the reference current 629, the reference current 629 is determined by a potential of a nodal point 620 and a resistance value of a resistance element 621 in Figure 62. Furthermore, the potential of the nodal point 620 can be changed by means of a control data signal line 628 by a voltage adjustment portion 625. To be more specific, it is possible, by controlling the control data signal line 628 with 641, to change it within the range determined by the resistance value of the resistance element 621.

Please replace the paragraph at page 122, lines 14-19, with the following rewritten paragraph:

In the case of displaying the moving image ~~for use~~ as previously described, it is desirable to collectively insert black to clarify the contours, and besides, it is also desirable to collectively insert black in view of the power for the gate driver circuit of driving the organic EL display apparatus.

Please replace the paragraph at page 122, line 20, to page 123, line 6, with the following rewritten paragraph:

The gate driver IC 12 of driving the EL display panel operates each gate signal line 17b by means of a shift register 61b of operating the start pulse ST2 on a clock CLK2. In the case of collectively inserting black for use shown in 781, each gate signal line 17 has only to be turned on and off once in one inter-frame space. In the case of dividedly inserting black

~~for use~~ as shown in 782, the gate signal lines 17 are repeatedly turned on and off. For this reason, multiple signal lines are simultaneously turned on and off, and so there is a problem that power consumption of the gate driver IC 12 is increased.

Please replace the paragraph at page 123, lines 7-23, with the following rewritten paragraph:

From the above viewpoints, it is preferable that the organic EL display apparatus collectively insert black under ordinary circumstances. In the case of collectively inserting black, however, the flicker due to collectively inserting black on the still image is visible. The still image or the video with little movement is displayed for that reason. Figures are schematic diagrams of the display state of the mounted panel according to the present invention. Figures are schematic diagrams of the display state of the mounted panel according to the present invention. In this case, it requires a mechanism of changing the collective insertion of black to the divided insertion of black. However, if switched from the collective insertion of black to the divided insertion of black, the flicker is seen at the moment of switching. There are two thinkable reasons for this.

Please replace the paragraph at page 125, line 4, to page 126, line 3, with the following rewritten paragraph:

The present invention proposes a method of solving the two problems and changing the method of inserting black from the collective insertion to the divided insertion without deterioration of the image. The deterioration of the image on switching is caused by rapid change in the luminance and feeling of black as previously described. Therefore, according to the present invention, the deterioration of the image on switching is prevented by the method of gradually dividing the interval of black over multiple frames ~~for use~~ as shown in

Figures 89. Figures 80 show the change in the luminance in the case of making the intervals of N horizontal scanning periods (hereafter, the horizontal scanning period is described as H) and dividing the number of lit-up horizontal scanning lines into two. In a status of having S pieces of the horizontal scanning lines lit up, a preceding stage of the start pulse divided in two is 801 and a subsequent stage thereof is 802. Then, the number of lit-up horizontal scanning lines of 801 and 802 is S/2 (S = 2·4·6 ... ·). For this reason, after the start pulse 801 of the preceding stage is outputted to the gate signal line, the number p of horizontal scanning lines having the EL display panel lit up during S/2 (H) is (S/2) – N pieces. The luminance of the display panel during that time is as follows against that before switching.

Please replace the paragraph at page 128, line 19, to page 129, line 12, with the following rewritten paragraph:

The circuit 854 is the circuit of dividing and outputting the waveform from the lighting rate control value and the value of the counter 554 shown in Figure 73, which is reconfigured as the circuit having less delay. The circuit of Figure 73 is the same as 854, and either one may be used. The circuit 853 renders the output 856 HI when the counter 851 is 0. It also generates a counter value of rendering the output 856 LOW from the lighting rate control value in the additional value control circuit 855. In the case where the lighting rate control value is N bits and the start pulse ST2 to be inputted to the gate driver circuit IC 12 is divided into 2 raised to t-th power, the output 856 is rendered LOW when it becomes the value of a high-order (N – t) bits of the lighting rate control value. The counter 851 is set ~~for use~~ to be initialized to 0 by the value at which all (N – t) bits become 1. When initializing the counter 851, the selector 858 is controlled to select the output 857 from the circuit 854.

Please replace the paragraph at page 131, line 14, to page 134, line 20, with the following rewritten paragraph:

Subsequently, a description will be given as to a circuit configuration of gradually changing the insertion interval of black, which uses an additional value control apparatus. The additional value control apparatus 855 is used to simultaneously control the two counters 851 and 852. The additional value control apparatus 855 uses a state of adding one by one, a state of adding the lighting rate control value and a division number of the waveform or the value derived from the insertion interval of black, and a state of adding nothing according to the circumstances so as to control the insertion interval of black. Changes in the state of the additional value control apparatus will be described by referring to Figure 87. Reference character Y denotes a value of initializing the counter 851, and X denotes a value of rendering the output 856 LOW. Reference numeral 8701 denotes a vertical synchronizing signal, 8702 denotes a start pulse in a collective black insertion state, 8703 denotes a state in which insertion interval of black 8704 in the preceding stage is N (H), 8705 denotes a state in which the insertion interval of black 8704 in the preceding stage and insertion interval of black 8706 in the subsequent stage are almost the same intervals. As the aforementioned image deterioration occurs if it is changed from the state of 8703 to the state of 8705, the aforementioned insertion interval of black 8704 is gradually extended such as N, 2N, 3N and so on, and are eventually put in the state of 8705 so as to prevent the image deterioration. A description will be given by using the graph of Figure 87 as to operation of the additional value control circuit 855 in the state of 8703. The broken line indicated by 8707 is the graph of the values of the counter in the case where the counters 851 and 852 rise one by one. In comparison, a graph 8708 indicated in full line is the graph of the values of the counter, where increased values of the counters 851 and 852 are controlled by the additional value control circuit 855. The additional value control circuit 855 controls the counters 851 and

852 to increase one by one until the value of the counter 851 becomes X. And the start pulse becomes LOW when the value of the counter 851 becomes X. Originally, the start pulse becomes HI next at the time of Y when the counter 851 is initialized, and there should be a Y – X (H) period in between. Here, the additional value control apparatus 855 exerts control so that the counters 851 and 852 become the value of Y – N by adding a value as indicated by 8709. Thus, the period until the start pulse becomes HI next is reduced to N (H). Here, the additional value control apparatus 855 returns the value to be added to the counters 851 and 852 to 1 as indicated by 8710. The counters 851 and 852 have their values reach Y after N – 1 (H). The period until reaching the value of Y changes depending on how the value of 8709 is added. In the case where the value of 8709 is asynchronously ~~performed~~ added to the counter 851, there is a possibility that the period until reaching the value of Y may become N (H). The present invention may use either way of addition. And then, the counter 851 is initialized and the output 857 is selected, and the start pulse becomes HI again thereafter. Thus, the insertion interval of black 8704 in the preceding stage becomes N (H). The start pulse becomes LOW again X (H) after it became HI. Here, as indicated by 8711, the additional value control apparatus 855 exerts control to put the counters 851 and 852 in no addition state in order to render the values of the counters 851 and 852 equal to the value of 8707. The values of the counters 851 and 852 become equal to the value of 8707 by continuing the no addition state for the same period as the value added to the period of 8709. If the values of the counters 851 and 852 become equal to the value of 8707, the additional value control apparatus 855 returns the increased values of the counters 851 and 852 to 1. Figure 88 shows a variation diagram of the counters 851 and 852 when changing from the division into two to division into four, and Figures 89 show the change in the insertion interval of black in that case. From Figures 89, it is understandable that it is a feasible, by using the above driving method, to implement the driving method of gradually adjusting the

insertion interval of black, which has solved the problems of the image deterioration due to the rapid change in the luminance and the image deterioration due to the rapid change in the insertion interval of black.

Please replace the paragraph at page 148, lines 3-17, with the following rewritten paragraph:

A measurement period of accumulable data, that is, the amount of current changes according to the capacity of the FIFO memory. As shown in Figure 104, a time until saturation of the temperature rise of the device~~, time until saturation~~ changes according to light emission area. It takes one minute in the case where the light emission area is small, and it takes ten minutes in the case where the light emission area is large. For that reason, it is necessary to prepare a memory capable of grasping the current values between the present and 1 to 10 minutes in the past. The time until saturation of the current also changes according to the size of the device, radiation conditions and materials of the organic EL element, and so it may be necessary to grasp the current values for a longer time depending on the conditions.

Please replace the paragraph at page 148, line 18, to page 150, line 14, with the following rewritten paragraph:

Next, a method of controlling the amount of current will be described by referring to Figure 105. As previously described, the present invention manipulates the number of lit-up horizontal ~~operating~~ scanning lines from the video data and thereby controls the lighting time so as to suppress the amount of current. As a method of controlling the number of lit-up horizontal ~~operating~~ scanning lines from the video data, a maximum number of lit-up horizontal ~~operating~~ scanning lines 1050 and a minimum number of lit-up horizontal

~~operating~~ scanning lines 1051 are inputted to a lighting rate control circuit 1054. Calculation is performed from these two points to derive the relation between the video data and the number of lit-up horizontal scanning lines, and output data 1053 is outputted according to input data 1052. As for the method of calculation, the difference between 1050 and 1051 should be taken and divided by the division number according to the video data so as to acquire the inclination. In this case, the relation becomes proportional if the difference between 1051 and 1050 is equally divided as in 1060, and it is also possible to draw a curve by weighting and dividing it as in 1061. As shown in Figure 107, the present invention suppresses the current by using a circuit 1070 of controlling 1050 and 1051 with an output value of 1024. 1071 inputted to 1070 is intended to input a boundary value of whether or not to suppress the current. In the case where the output from 1024 is larger than 1071, the current is suppressed. In the case where the output from 1024 is smaller than 1071, the current is not suppressed. Suppression of the current is performed by manipulating the maximum number of lit-up horizontal ~~operating~~ scanning lines 1050 and the minimum number of lit-up horizontal ~~operating~~ scanning lines 1051 ~~for use~~ as previously described. In the case where the output from 1024 is larger than 1071, the current is suppressed by outputting 1072 and 1073 to which the values have been reduced from the inputted maximum number of lit-up horizontal ~~operating~~ scanning lines 1050 and minimum number of lit-up horizontal ~~operating~~ scanning lines 1051. As for the method of reduction, there is a method of reducing them by a fixed amount in the case of exceeding 1071 or a method of calculating the difference between the output of 1024 and 1071 and reducing them by that value. The latter can minutely control a suppression amount of current so as to improve the accuracy of the suppression amount. In the case of controlling 1051 and 1050, it is not necessary to reduce them by the same value. A method of reducing only 1050 is also thinkable as in Figure 108.

Please replace the paragraph at page 150, lines 15-22, with the following rewritten paragraph:

Figure 109 shows the relation between the number of lit-up horizontal ~~operating~~ scanning lines and the video data in the case of controlling the maximum number of lit-up horizontal scanning lines 1050 and the minimum number of lit-up horizontal ~~operating~~ scanning lines 1051, and the relation of the amount of current passing through the device against the video data in the case of controlling them.

Please replace the paragraph at page 161, line 15, to page 162, line 13, with the following rewritten paragraph:

As for the method of reducing the amount of data, there is a method of reducing the amount of data by converting the gamma curve of expanding the input data as shown in Figure 126. The gamma curve conversion is conducted by using a gamma curve conversion circuit having a few break points. As shown in Figure 126, the break points when suppressing no amount of current are denoted by reference characters 1261a, 1261b, ... 1261h. As opposed to them, points for reducing the data are provided, such as 1262a, 1262b, ... 1262h. A line connecting the respective break points is decomposed by a current suppression value 1264 and reconnected to allow the gamma curve such as 1263 to be generated. And it is thereby possible to uniformly reduce the entire data without collapsing the ratio of the output data to the input data. The values of 1262a, 1262b, ... 1262h should preferably be 0. It is because, in the case where 1262a, 1262b, ... 1262h are 0, it is only necessary to divide the values of 1261a, 1261b, ... 1261h by a control value. However, the present invention does not limit the values of 1262a, 1262b, ... 1262h to 0. If the values of 1262a, 1262b, ... 1262h are set at 1/2 of the values of 1261a, 1261b, ... 1261h, it becomes

possible to place a limit so that the current value can only be reduced to 1/2 whatever control is exerted.

Please replace the paragraph at page 164, line 3, to page 165, line 2, with the following rewritten paragraph:

Figure 128 shows the circuit configuration of implementing the present invention. 1281 has a mechanism of calculating the data inputted from outside and judging a video status. 1282 has a mechanism of controlling the amount of current by means of the data outputted from 1281. 1283 has a mechanism of generating ~~from~~ the gamma curve. The gamma curve generated by 1283 is inputted to a gamma conversion circuit 1284. Input data RGB is converted by the gamma conversion circuit ~~1294~~ 1284 and is inputted to the source driver 14. 1285 has a mechanism of allocating the output of 1282 to the control of the number of lit-up horizontal scanning lines and the control of the gamma curve. The control value of the number of lit-up horizontal scanning lines is inputted to the gate driver circuit IC 12, and the control value of the gamma curve is inputted to 1283. In the case where the output of 1282 is to control the entire amount of current to 1/4, 1285 then converts to control the number of lit-up horizontal scanning lines to 1/2 and also converts to control the gamma curve to 1/2. Thus, the entire amount of current becomes 1/4. It is possible to implement various current suppression methods by changing in 1285 the ratio of allocation to the control of the number of lit-up horizontal scanning lines and the control of the gamma curve.

Please delete the heading at page 177, line 13, as follows:

~~Industrial Applicability~~